atent No. 7,158,568 B2

PU020119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

blicant

: Jepngsoon Park, Seo Weon Heo, Ivonete Markman, Saul Brian Gelfand

Serial No.

: 10/511,387 : 10/15/04

Filed For

: EQUALIZER/FORWARD ERROR CORRECTION AUTOMATIC MODE

SELECTOR

Examiner

: Emmanuel Bayard

Art Unit

: 2611 Customer No.: 24498

REQUEST FOR CERTIFICATE OF CORRECTION

Chief Information Office U.S. Patent and Trademark Office Alexandria, VA 22313-1450

Sir:

It is respectfully requested that a Certificate of Correction be issued under the provisions of Rule 322 to correct errors in the above-identified patent. The corrections to be made are stated on the enclosed PTO/SB/44 form.

The submitted declaration misspelled the inventor's last name. However, the inventor correctly signed the declaration. This was the fault of the applicant.

Accordingly, it is respectfully requested that a Certificate of Correction be issued as indicated on the enclosed PTO/SB/44 form.

Please charge any fees related to this request to Deposit Account 07-0832.

Respectfully submitted,

By:

Reg. No. 36,229

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Enclosures (Form PTO/SB/44 & Filing Receipt)

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO: 7,158,568 B2

DATED: January 2, 2007

INVENTOR(S): Jeongsoon Park, Seo Weon Heo, Ivonete Markman, Saul Brian Gelfand

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the first page of the patent, please correct the Inventor's name "Markman Ivonete" to --Ivonete Markman---

MAILING ADDRESS OF SENDER:

J. J. Opalach Thomson Licensing LLC P. O. Box 5312, Princeton, NJ 08543-5312

PATENT NO. 7, 158, 568

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



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(12) United States Patent

Park et al.

(10) Patent No.:

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(45) Date of Patent:

Jan. 2, 2007

(54) EQUALIZER/FORWARD ERROR CORRECTION AUTOMATIC MODE SELECTOR

(75) Inventors: **Jeongsoon Park**, Lafayette, IN (US); **Seo Weon Heo**, South Korea (KR);

Voncte Warkman Ivonete. Carmel, IN (US): Saul Brian Gelfand, Lafayette. IN

(US)

(73) Assignee: Thomson Licensing.

Boulogne-Billancourt (FR)

(*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35

U.S.C. 154(b) by 162 days.

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10/511,387

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Apr. 10, 2003

(86) PCT No.:

PCT/US03/11207

§ 371 (c)(1),

(2). (4) Date: C

Oct. 15, 2004

(87) PCT Pub. No.: WO03/090389

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(65) Prior Publication Data

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Related U.S. Application Data

- (60) Provisional application No. 60/373,205, filed on Apr. 17, 2002.
- (51) **Int. Cl.** *H03H 7/30*

(52)

(2006.01)

See application file for complete search history.

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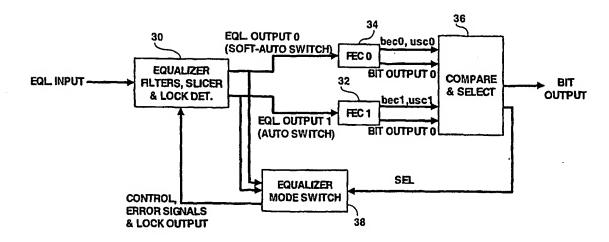
* cited by examiner

Primary Examiner—Emmanuel Bayard (74) Attorney, Agent, or Firm—Joseph J. Laks; Ronald H. Kurdyla; Joseph J. Opalach

(57) ABSTRACT

An apparatus for automatically selecting one of a standard decision directed mode and a soft dd mode in a decision feedback equalizer for receiving a data signal includes an equalizer utilizing forward error correction for providing first and second output signals corresponding to a DFE automatic switching mode and a soft automatic switching mode, respectively, and a comparator for comparing byte error rates of the first and second output signals for selecting as a superior mode that mode associated with a lower ByER and outputting the output signal with the lower ByER. A lock detector provides a lock signal derived from the DFE output signal with the lower ByER and a mode switch selectively places the DFE outputs in one of the dd modes or a blind mode, depending on the lock signal.

25 Claims, 4 Drawing Sheets



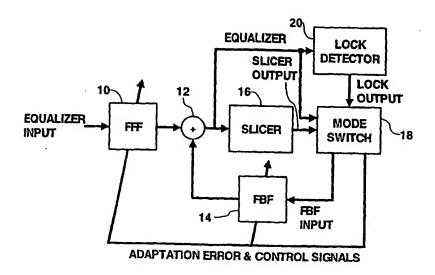


Fig. 1

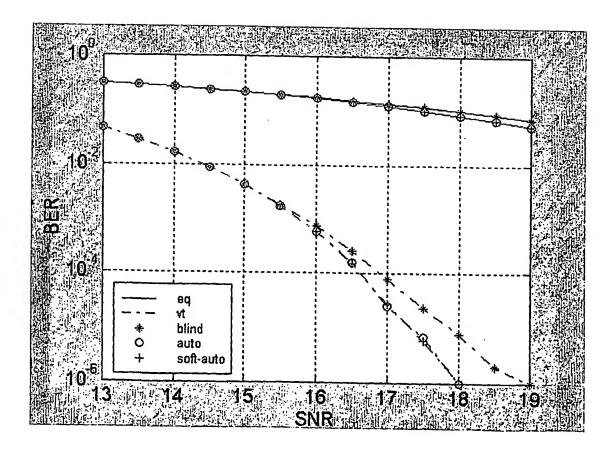


Fig. 2